28.2 A Spatial-Temporal Multi-Resolution CMOS Image Sensor with Adaptive Frame Rates for Moving Objects in the Region-of-Interest

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For fast-moving objects, high-speed image capturing is important to obtain sharp images without motion-blur. However, high frame-rate images of high spatial resolution require a large bandwidth and large power consumption, which is not feasible for bandwidth-limited applications such as wireless sensor networks. One way to reduce the bandwidth is to provide multiple temporal resolutions; specifically, to retain a high frame rate only in the region-of-interest (ROI) where the fast moving objects are located and allow a slow frame rate for stationary backgrounds. Additionally, spatial resolution can be further optimized to reduce the bandwidth. Therefore, in order to acquire an image with high resolution stationary backgrounds and negligible motion-blur in moving objects, it is desirable to implement a spatial-temporal multi-resolution sensor. Also, a motion detection function should be integrated on the sensor chip to provide a real-time identification of the ROI for moving objects. Several motion detection schemes have been reported, but their pixel size is large because they contain in-pixel capacitors to store the previous frame image [1, 2]. There are a few multiple-resolution sensors reported as well. However, none of them offered the combination of spatial-temporal multiple resolutions for the specific ROI [3, 4]. In this paper, we report on a CMOS image sensor that simultaneously generates spatial-temporal multiple-resolution readouts using two channels: one for low frame rate data at maximum spatial resolution for stationary backgrounds and the other for high frame rate data at low spatial resolution for moving objects in a specified ROI.

In normal operation, the proposed CMOS imager gives a 256×256 8b normal image. In the presence of motion, a 128×64 1b motion detection image is generated by the motion comparator by comparing the current frame with the previous frame. The motion data are used as the basis for setting the ROI in an external FPGA. The ROI address is accessed by a column selector and row decoders, and the 8b ROI image will be sent at a high frame rate. In ROI images, 4 pixels in a 2×2 array are spatially merged by charge summing in the floating diffusion (FD) of the shared pixels in order to achieve a high SNR image even with the short integration time that accompanies a high frame rate. Two CDS/ADC blocks allow simultaneous independent access to the ROI image in a 1/4-resolution image (2×2 pixels merged) at a high frame rate (>960fps) and images with full spatial resolution at the normal frame rate (<30fps) using separate output channels. These two images are combined in a multiple-resolution image containing all of the objects without any motion blur.

Figure 28.2.1 shows the block diagram of the sensor chip. Left and right row decoders select even and odd rows, respectively. The column selector enables independent pixel control for the ROI as well as for the background region (outside of the ROI). The top and bottom CDS/ADC blocks sample the signals from the even and odd columns, respectively. The chip has two channels for multiple-resolution readout: One is for normal image signals scanned by a shift register and the other is for ROI image signals selected by a decoder. Two counters are used for the single-slope ADCs. A bootstrapping block generates a voltage greater than $V_{DD} + V_{TH}$ for activating the inter-pixel switch. A motion comparator block derives 1b motion data from the frame difference.

Figure 28.2.2 shows the pixel and column architecture. Four pixels are shared and an inter-pixel switch (IS) is connected between the upper and lower FD nodes for motion detection. Transistor TX is enabled when both TX1(row) from the row decoder and TX1(Col) from the column selector are activated. Likewise, each pixel is reset when both Reset(Col) and Reset(Row) are activated. The signal is sampled by one of the CDS/ADC blocks. The switches are in position N for normal image capture and R for the ROI.

Figure 28.2.3 shows the operating procedures for motion detection. In order to maintain a small pixel size, we used FD as an analog memory instead of using in-pixel storage capacitors [5]. Four pixels are merged and two rows are read at a time. After reading the lower group signal, the inter-pixel switch IS is turned on and half of the charge is transferred into the upper FD. After IS is turned off, the upper FD stores the signal from the lower group for half of the integration time ($T_{INT}/2$). After $T_{INT}/2$, the previous frame signal (stored in the upper FD) is compared with a newly generated signal from the current frame. After another $T_{INT}/2$, the newly generated charge during the next $T_{INT}/2$ cycle will be added to the remaining charge in the lower FD and the combined signal will be read. This procedure will repeat. The timing diagram for multiple-resolution readout is also shown in Figure 28.2.3. During the one-row access time for normal readout, $2(K + 1)$ rows can be read in the ROI since the two rows are read simultaneously by pixel merging. K is dependent on the row access time for normal readout. When the normal readout rate is 15fps, K becomes 7 and the ROI image can be read at 960fps (a 64×64 ROI). Motion detection starts after the CDS for the ROI has been completed. The row address will change to $(R - X)$ where X is half the number of rows in the ROI since the motion detection starts every $T_{INT}/2$. After the ROI is assigned, motion detection is performed inside the ROI region. If motion is detected inside the ROI, then a new ROI will be defined according to the movement of the object. Unfortunately, true CDS cannot be performed because we used a p-n diode from the standard CMOS processes instead of a customized pinned photodiode.

Figure 28.2.4 shows the inter-pixel switch operation. In order to control the IS by both row decoders and a column selector, the BS transistor is added. This results in a $2V_{TH}$ drop across the transistors and the two FDs cannot be completely equalized by the IS. To resolve this problem, a bootstrapping circuit is employed to generate a voltage greater than $V_{DD} + V_{TH}$ to enable the IS. The output voltage of the bootstrapping circuit is given by $2(C_S/(C_S + C_L))V_{DD}$ [6]. Since one bootstrapping circuit drives the large parasitic capacitance in a row bus, we implemented a scheme to provide variable C_S and thus provided a customized output voltage for reliable IS control. In the column selector, a serial input is entered into a 128b shift register and then latched.

A prototype chip has been fabricated using a 0.35μm CMOS logic process. Figure 28.2.5 shows captured images from the fabricated device including a 256×256 normal image and a 128×64 1b motion image for a rotating wheel. The normal image with a rotating panel with a character M shows significant motion blur. This motion blur can be completely eliminated in a high frame-rate ROI image. The size of the ROI is set to 64×64 but it is controllable. From the two outputs, a 256×256 multiple-resolution image can be successfully constructed where the ROI image is expanded from 64×64 to 128×128 and brightness is adjusted. The performance of the sensor is summarized in Figure 28.2.6 and a chip micrograph is shown in Figure 28.2.7.

References:

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[2] U. Mallik et al., "Temporal Change Threshold Detection Imager," *ISSCC Dig Tech. Papers*, pp. 362-363, Feb., 2005.

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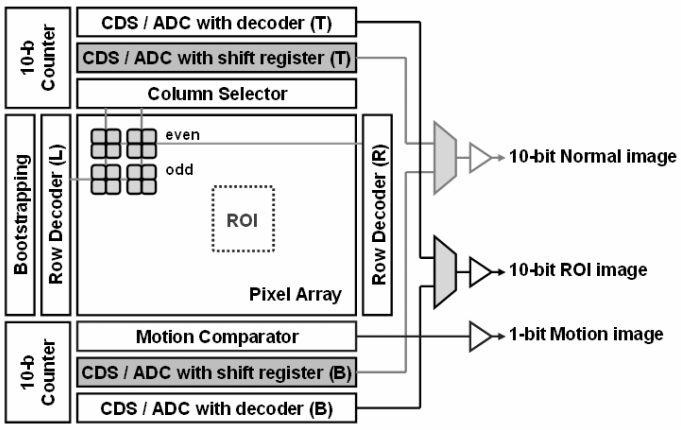

Figure 28.2.1: Chip block diagram.

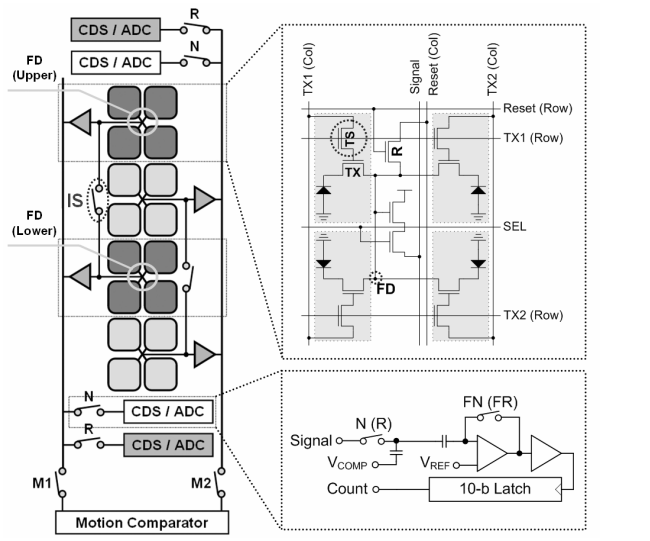

Figure 28.2.2: Pixel and column architectures.

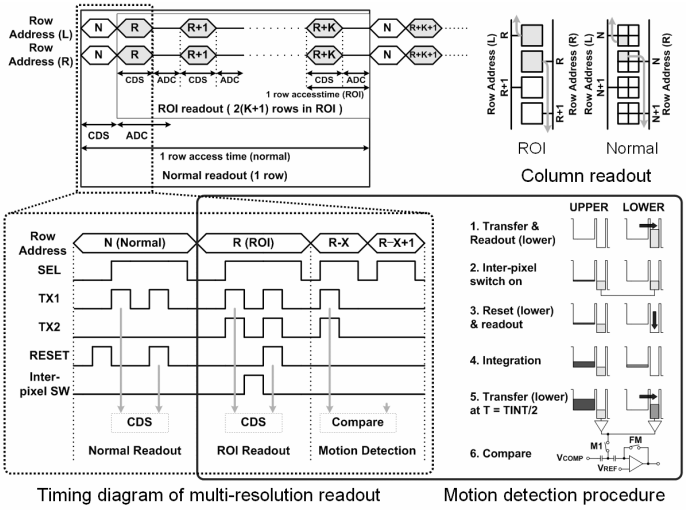

Figure 28.2.3: Operating procedures.

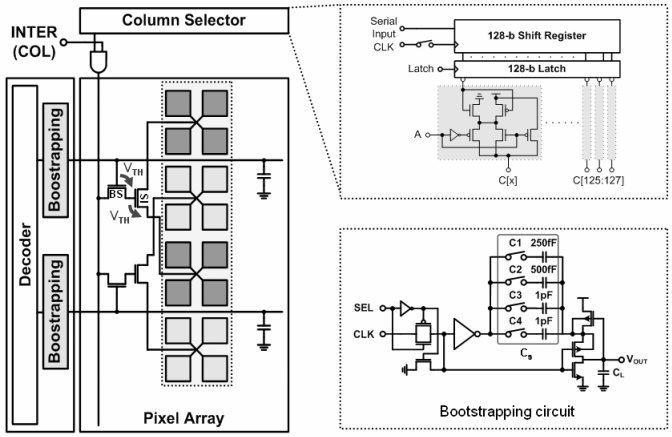

Figure 28.2.4: Architecture and circuits for inter-pixel switch control.

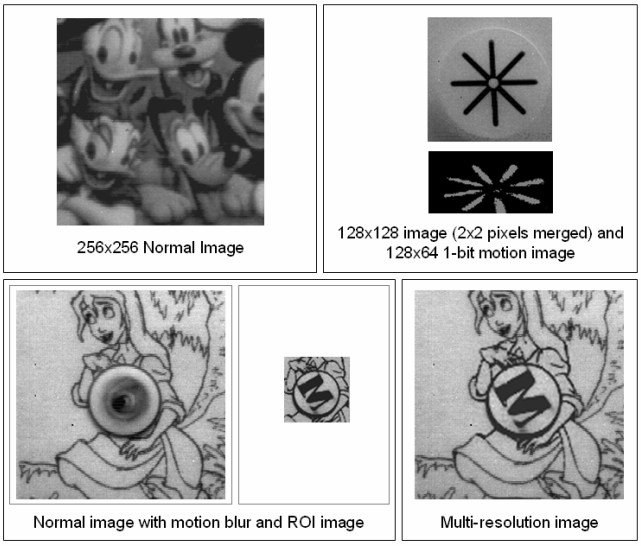

Figure 28.2.5: Sample images from the fabricated chip.

Technology	0.35μm 1P4M CMOS logic
Die size	5 x 5mm
Array size	256 x 256
Photodiode	n+/psub
Pixel size	8.9 x 8.9μm
Number of transistors per pixel	3T
Fill factor	27%
Dark signal	24.7mv/sec
Frame rate	< 30 fps for 8-b normal image
	> 960 fps for 8-b ROI image (@ 64×64 ROI, size is controllable)
Supply voltage	3.3 V
Power consumption	74.87mW in multi-resolution readout (@ 30fps normal / 240 fps 64 x 64 ROI)

Figure 28.2.6: Chip characteristics.

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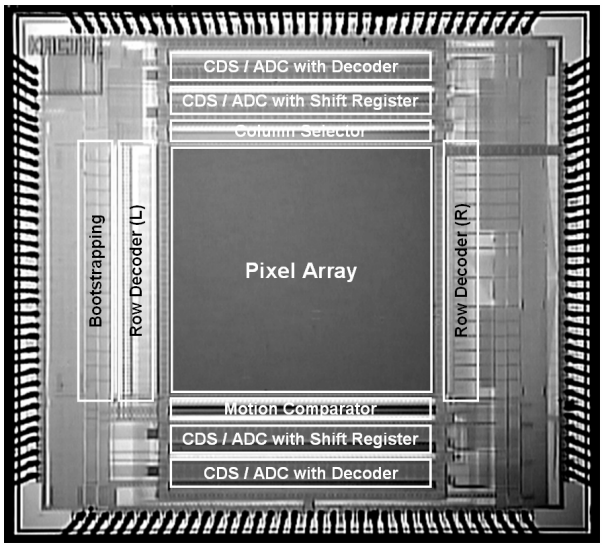

Figure 28.2.7: Chip micrograph.

